

**IN THE DRAWINGS:**

The attached sheets of drawings include changes to Figs. 2, 4A-E, 5A-D, 6A-C, 12A, 21A, and 23 to correct informalities therein. These sheets replace the original sheets containing these drawings. Applicants are also submitting formal drawings herewith.

Attachment: Replacement Sheets

Annotated Sheets Showing Changes

### REMARKS


When preparing formal drawings, Applicants noticed a few minor informalities in the claims, including misspellings. Applicants are correcting these informalities herein. No new matter is being added. Therefore, it is respectfully requested that these amendments be entered and allowed.

If any fee is necessary for this submission or amendment, please charge our deposit account 50/1039.

Favorable consideration is earnestly solicited.

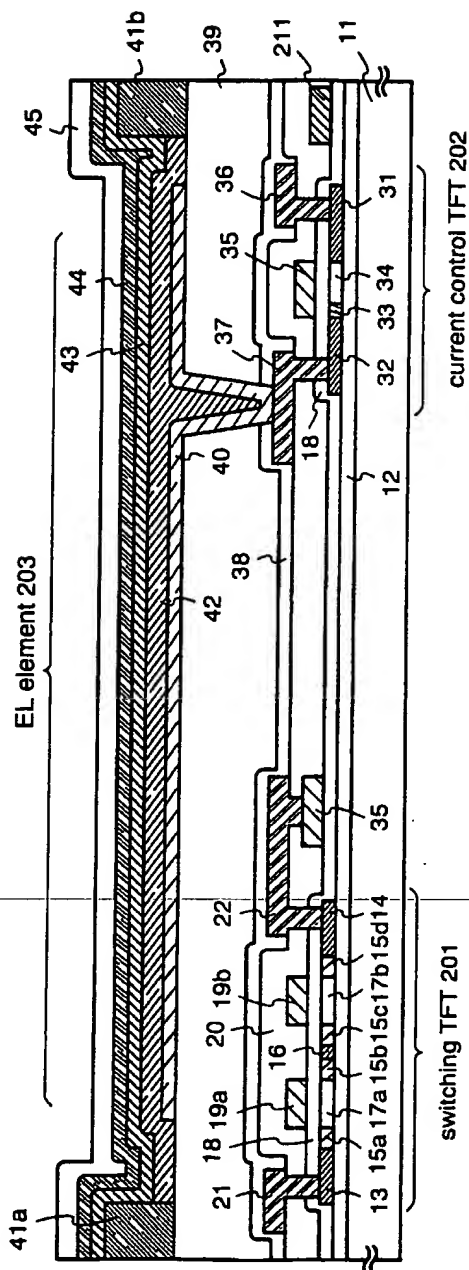
Date: *March 9, 2007*

Respectfully submitted,

  
Mark J. Murphy  
Registration No. 34,225

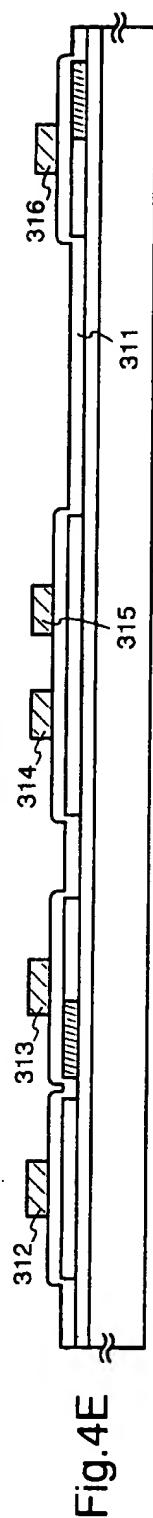
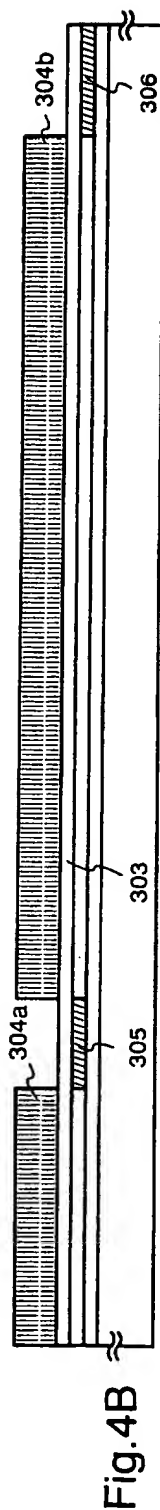
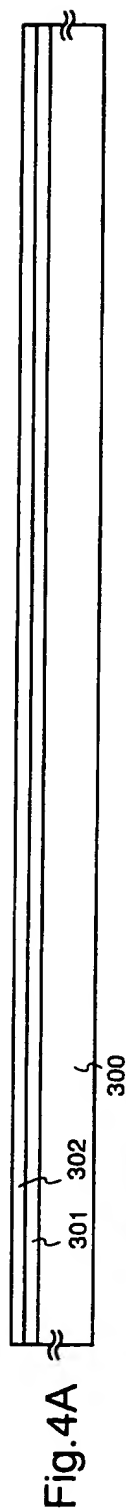
COOK, ALEX, McFARRON, MANZO,  
CUMMINGS & MEHLER, LTD.  
200 West Adams Street  
Suite 2850  
Chicago, Illinois 60606  
(312) 236-8500

Customer no. 26568



- 11: substrate 12: base film 13: source region 14: drain region 15a-15d: LDD regions  
16: high concentration impurity regions 17a, 17b: channel forming region  
18: gate insulating film 19a, 19b: gate electrodes 20: first interlayer insulating film  
21: source wiring 22: drain wiring 23: gate electrode 31: source region 32: drain region  
33: LDD region 34: channel forming region 35: gate electrode 36: source wiring  
37: drain wiring 38: first passivation film 39: second interlayer insulating film  
40: pixel electrode (cathode) 41: bank 42: light emitting layer 43: hole injection layer  
44: anode 45: second interlayer insulating film

Fig.2



300: glass substrate 301: base film 302: polysilicon film 303: protective film 304a-304b: resist mask  
 305, 306: n-type impurity regions 307-310: active layers 311: gate insulating film 312-316: gate electrodes

polysilicon

resist

impurity

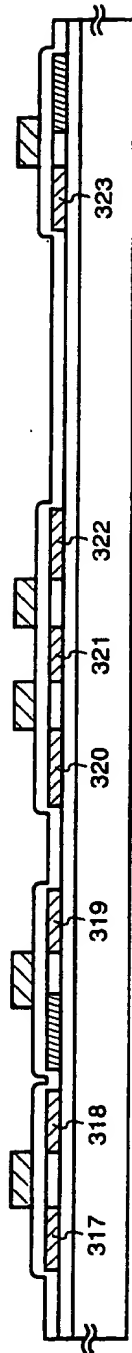


Fig. 5A

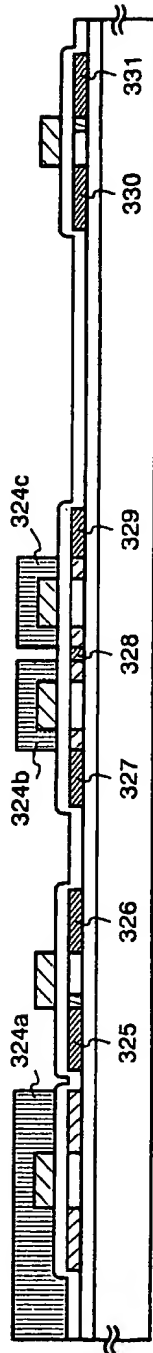


Fig. 5B

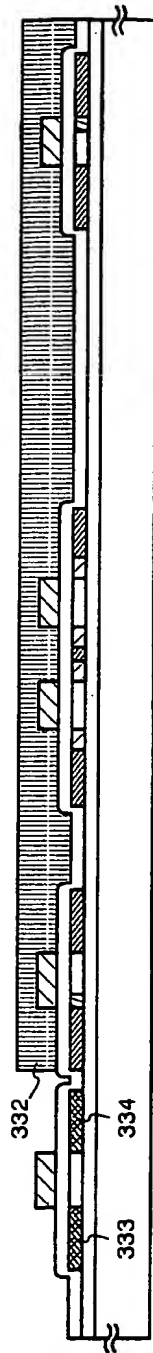


Fig. 5C

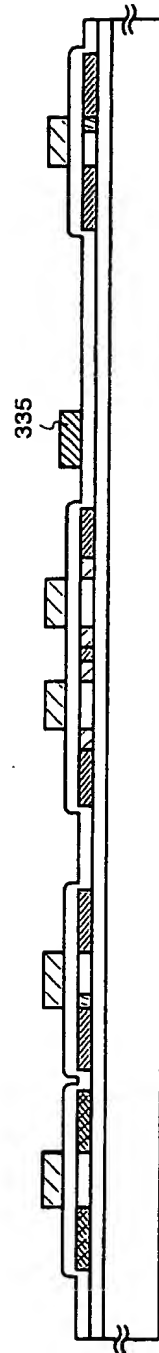


Fig. 5D

317-323: n-type impurity regions 324a-324c, 332: resist mask 325-331: n-type impurity regions  
333, 334: p-type impurity regions 335: gate wiring  
resist

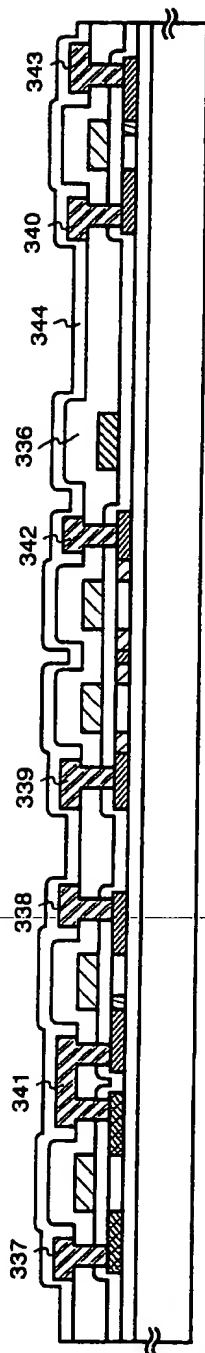


Fig. 6A

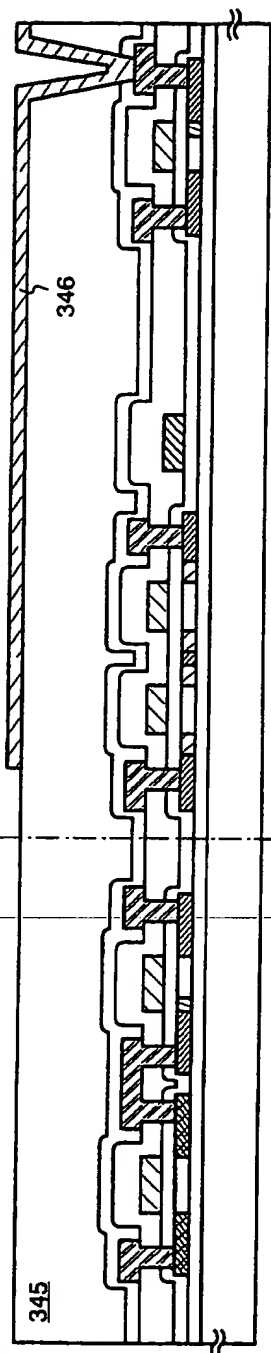


Fig. 6B

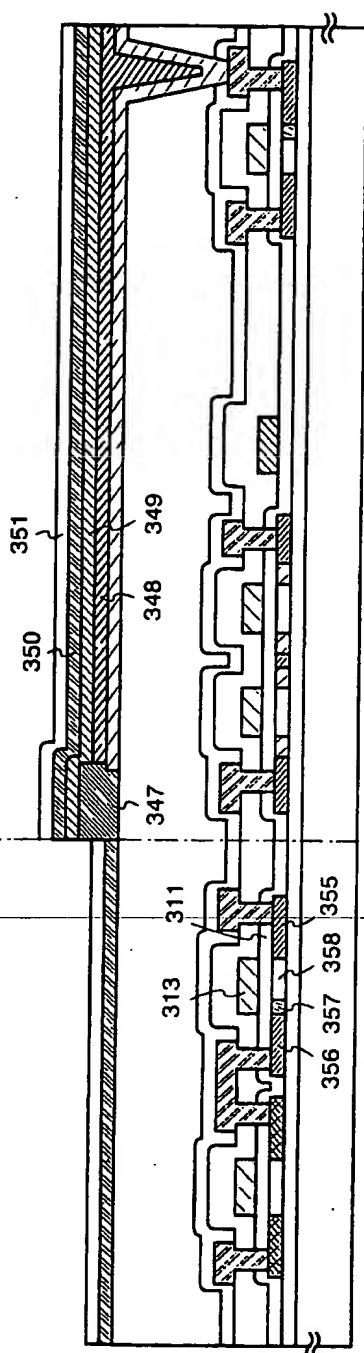


Fig. 6C

p-channel type TFT206 n-channel type TFT205 switching TFT201 current control TFT202

336: first interlayer insulating film 337-340: source wiring 341-343: drain wiring  
 344: first passivation film 345: second interlayer insulating film 346: pixel electrode (cathode)  
 347: bank 348: light emitting layer 349: hole injection layer 350: anode 351: second passivation film

cathode

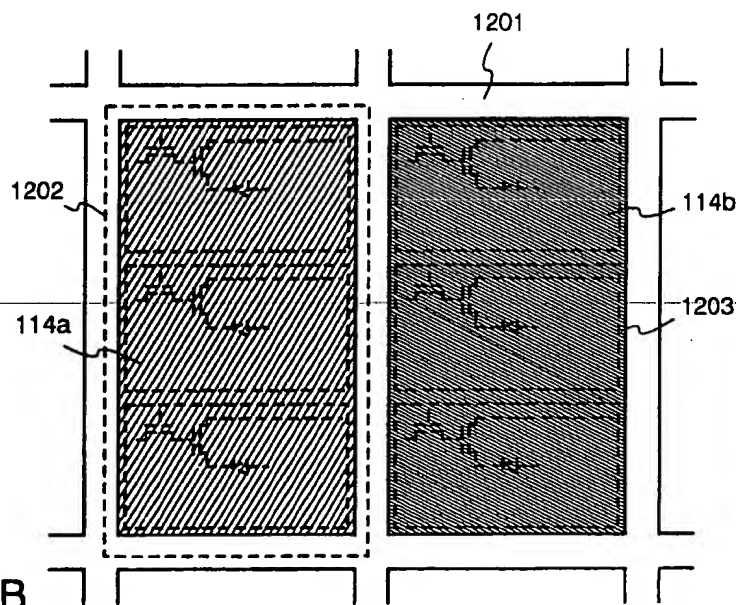
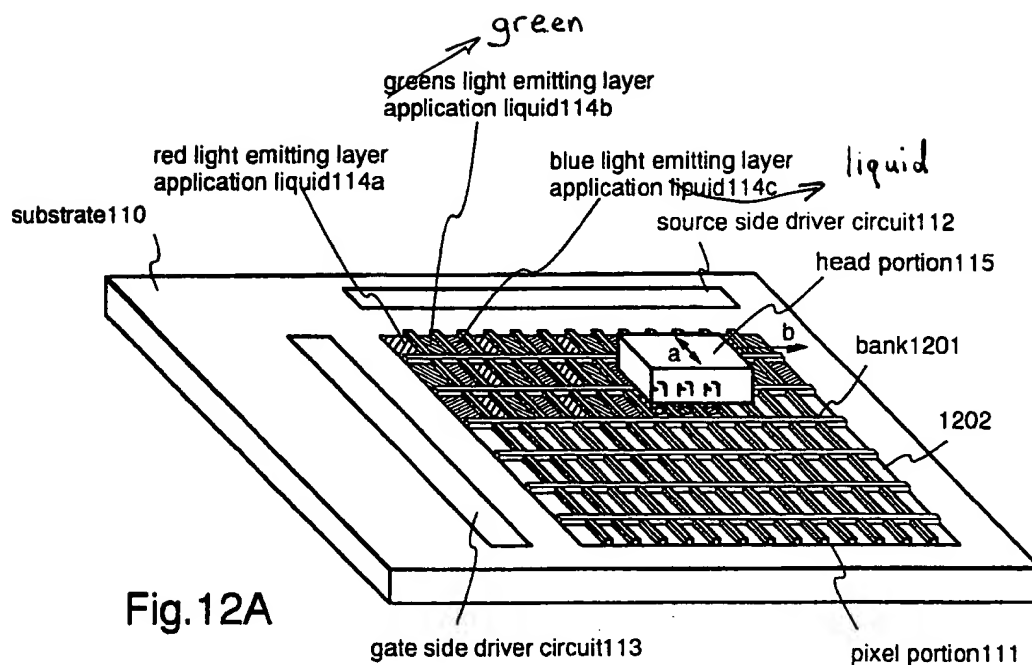


Fig.21A

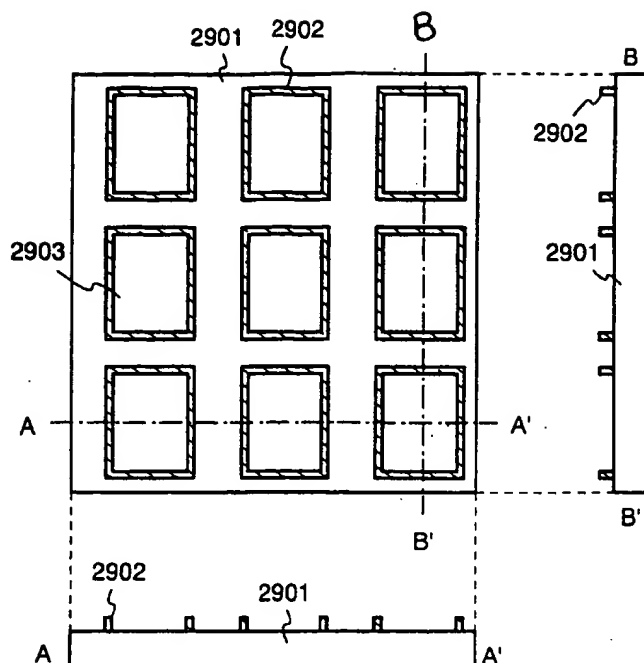
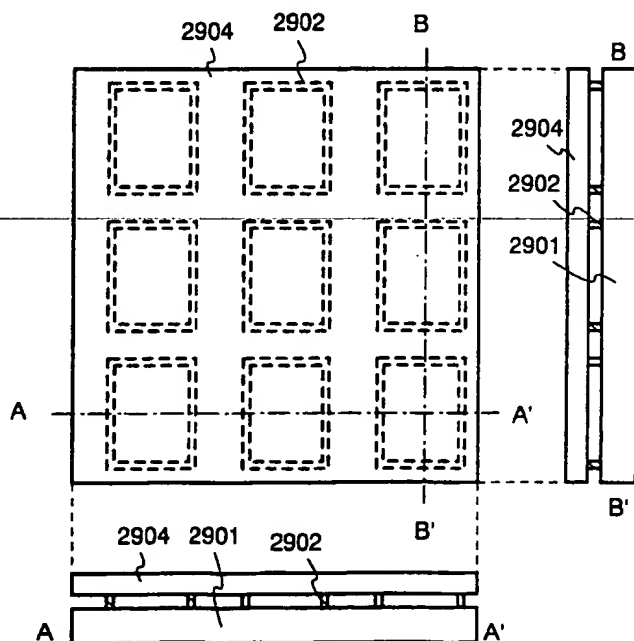


Fig.21B





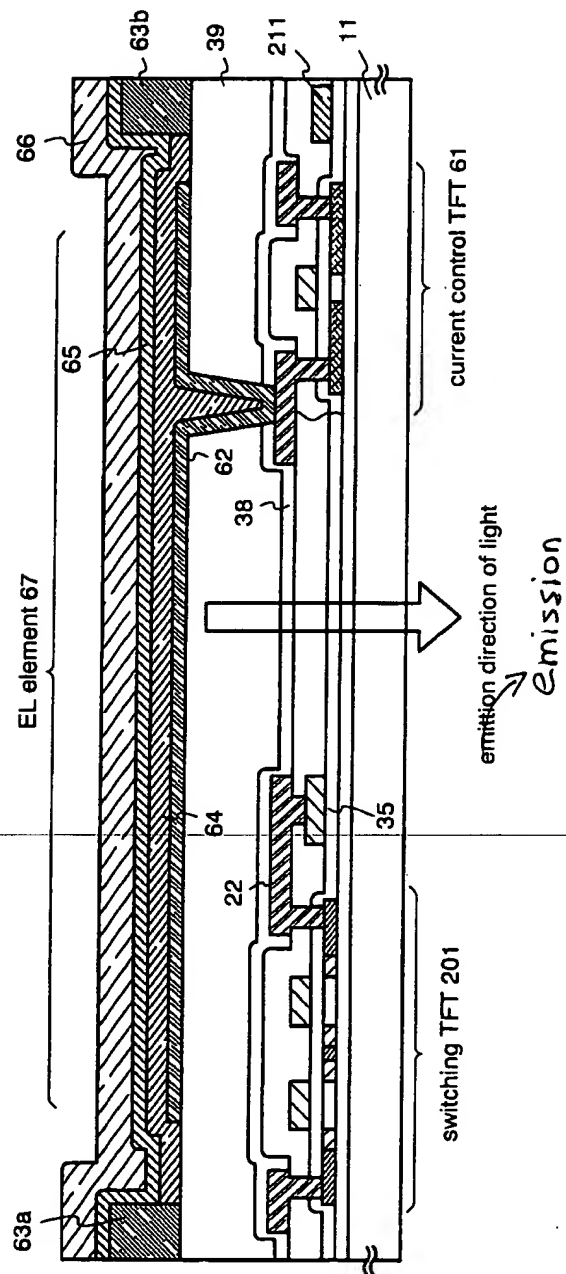


Fig.23